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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,282	04/21/2004	Keiichi Kushida	252121US2S	6377

22850 7590 01/17/2007

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,282	KUSHIDA ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 April 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/30/04, and 4/21/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 are presented for examination.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 8/30/04, and 4/21/04 have been considered by the examiner. Forms 1449 have been signed and returned with this office action.

Drawings

The drawings received on 4/21/04 are acceptable.

Claim Objections

Claims 6 and 7 are objected to because of the following informalities: The use of the term "if" causes questions of 35 USC 101 issues because there is no statement of what happens 'if not'. Therefore, the examiner will interpret this to be 'when' for purposes of examination. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of

an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Solt et al. U.S. Patent No. 6,988,237.

As per claim 1 Solt et al. teach the claimed semiconductor device comprising: a data memory which stores data (fig 5 element 122); a code memory which stores an error checking and correcting code (ECC code) corresponding to the data (fig 5 element 120); and an error checking and correcting unit (ECC unit) which outputs, to the data memory as the data, a test pattern required to test the data memory (figure 5 element 108), and which generates, from the test pattern, code information having an error checking function (fig 5 element 506), and outputs the code information to the code memory as the error checking and correcting code. (Column 2 lines 8-23)

As per claim 2, Solt et al. teach a test unit which simultaneously tests the data memory and the code memory by reading the test pattern written in the data memory and the code information written in the code memory. (Column 4 line 61 through column 5 line 1)

As per claim 3, Solt et al. teach the ECC unit checks an error on the basis of the code information read from the code memory, and the test unit tests the data memory and the code memory on the basis of results of the error check. (Column 5 lines 1-15)

As per claims 4 and 5, Solt et al. teach the ECC unit generates the code information using a Hamming matrix configured so that a sum of row components of the

matrix is odd. (Column 4 lines 14-20 – note: the ability to configure the sum of row components to be odd or even is inherent in the Hamming code)

As per claims 6 and 7 Solt et al. teach using all bits of the test pattern are "1"s, the ECC unit generates the code information so that all bits of code information generated from the test pattern are "1"s. (column 5 lines 29-37)

As per claims 8- 13 Solt et al. teach that when each memory line is analyzed individually, for example, as it is read from the memory, a more complex set of patterns is required. One such pattern is described below. This pattern requires log.sub.2 (bus_size) pairs of vectors, where bus_size is the width of the bus in bits. In the nth vector pair of the test pattern, the bit values alternate every n bits. The vectors in a pair differ by being shifted n bit places relative to each other. For example (coded example col 5 and 6) see, the first vector pair comprises 4'b0101 and 4'b1010, the second vector pair comprises 4'b0011 and 4'b1100, and so on. These vectors need not be presented in order, and can be shifted by a number of bits, as long as all of the vectors are shifted by the same number of bits, and in the same direction. (Column 5 lines 38-50)

As per claim 14 Solt et al. teach the claimed method of memory test which is applied to a semiconductor device including a data memory which stores data (fig 5 element 122) and a code memory which stores an error checking and correcting code (ECC code) corresponding to the data(fig 5 element 120), the method comprising:

generating a test pattern required to test the data memory (fig 5 element 506); outputting the test pattern to the data memory; generating, from the test pattern, code information having an error checking function, and outputting the code information to the code memory as the ECC code (figure 4); and simultaneously testing the data memory and the code memory by reading the test pattern written in the data memory and the code information written in the code memory. (Column 2 lines 8-23, Column 4 line 61 through column 5 line 1)

As per claims 15-17, Solt et al. teach that when each memory line is analyzed individually, for example, as it is read from the memory, a more complex set of patterns is required. One such pattern is described below. This pattern requires log.sub.2 (bus_size) pairs of vectors, where bus_size is the width of the bus in bits. In the nth vector pair of the test pattern, the bit values alternate every n bits. The vectors in a pair differ by being shifted n bit places relative to each other. For example (coded example col 5 and 6) see, the first vector pair comprises 4'b0101 and 4'b1010, the second vector pair comprises 4'b0011 and 4'b1100, and so on. These vectors need not be presented in order, and can be shifted by a number of bits, as long as all of the vectors are shifted by the same number of bits, and in the same direction. (Column 5 lines 38-50)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt

Cynthia Britt
Primary Examiner
Art Unit 2138